

Electrical, Optical and Fluidic Through-Silicon Vias for Silicon Interposer Applications

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Abstract

Modern high-performance computing systems and data centers are implemented as many-core server systems. Current state of the art data centers have server racks with pluggable boards where each board has many multi-core processors and memory units. These boards are connected via electrical or optical cables. In such systems, communication bandwidth between the high-speed microprocessor cores and the memory is limited. To leverage full performance of these powerful chips, it is required to provide high memory bandwidth as well as effective power delivery and heat removal solutions. To address these challenges in high performance computing systems, we present a 3D packaging solution that includes a novel silicon interposer with electrical, optical, and fluidic (trimodal) interconnects and through-silicon vias (TSVs). The electrical TSVs in the silicon interposer enable power and signal delivery from motherboard to chips stacked on top of the interposer. The optical TSVs in the silicon interposer can provide ultra-high bandwidth communication between chips on different silicon interposers through motherboard level optical links. The fluidic TSVs enable a coolant to be routed from the motherboard to the chips on the silicon interposer. We have fabricated and characterized polymer-clad electrical TSVs (for low stress) with diameter that meets ITRS projections for high-performance computing systems. Using the same polymer used for the cladding of electrical TSVs, we have fabricated and characterized optical TSVs adjacent to electrical TSVs. Spin coating of the photodefinable polymer for electrical and optical TSVs is done in single step. Fabrication of fluidic TSVs can be done using the same cladding as that of the polymer-clad electrical TSVs without electroplating the copper. This leaves behind an empty polymer-clad via which can be used as a fluidic TSV.

I: Introduction

The performance of a processor is commonly measured as the number of instructions it processes per unit time. For high performance and utilization of the processor, the rate at which memory supplies instructions and data to the processor must match with the rate at which the processor is processing them. With the migration towards multi-core and multi-threading, the memory gap problem becomes more acute since now multiple processors on a single chip will increase the memory bandwidth demand. Thus, all the performance benefits of this processor cannot be fully leveraged because memory speeds are much slower compared to the processor speed [1, 2]. Fig. 1 shows scaling in processor frequencies and the memory speed over the past years. To solve this problem, we must improve the memory throughput and reduce the memory latency which includes interconnect delay in addition to memory access delay. This was quantified with analytical

simulations to determine the effect of increased memory bandwidth on a processor chip, and we see that performance increase is proportional to the available memory bandwidth. Fig. 2 shows that throughput increases from 96 BIPS (billion instructions per second) to 128 BIPS for a conventional processor when the available memory bandwidth is doubled from 50 GB/s to 100 GB/s. The reason for this is that for a fixed die size, when the available memory bandwidth is low, a larger cache is required to counter the effect of cache misses. Whereas, as the memory bandwidth increases, the cache size constraints are lowered thus allowing for more cores in the same area resulting in higher performance [3]. The performance improvement can be even higher for a 3D integrated processor since vertical TSVs can reduce the path length and thus improve the memory latency as well [4].

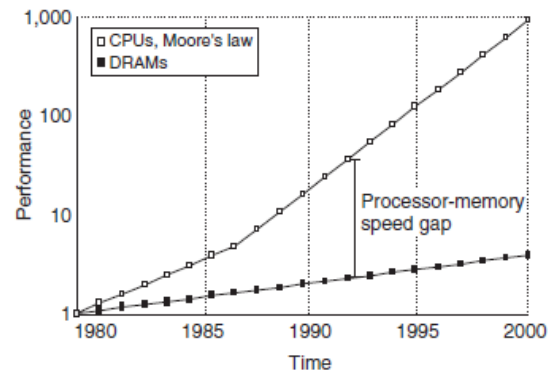


Fig. 1 Memory wall problem: Difference between the memory speed and the processor speed [2]

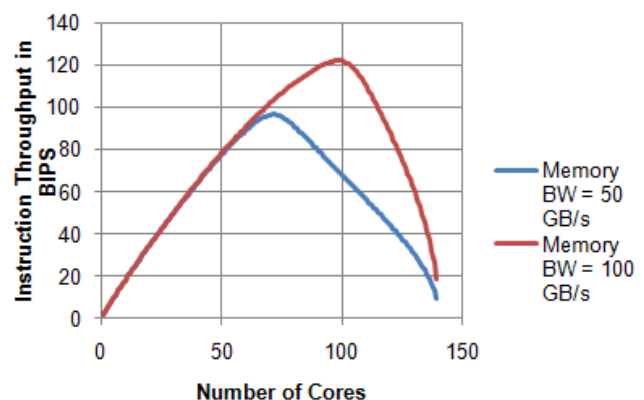


Fig. 2 Performance improvement in a many-core chip with high memory bandwidth (fixed die size)

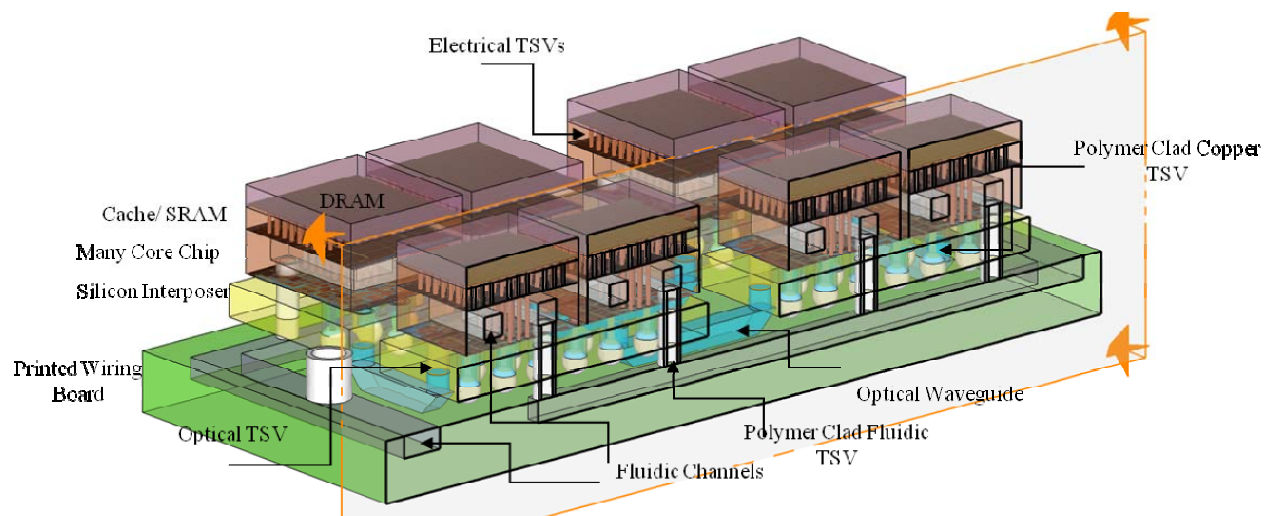


Fig. 3 Integrated trimodal interconnect system on silicon interposer

Optics is slowly and steadily replacing electric cables as a medium of communication. Optics is used almost for all long haul communication purposes. It has now come to wide use even in Local Area Networks (LANs). It has also found its way into supercomputers where the boards are connected via optical cables from the edge. Thus one of the approaches to solve the problem is to go down the path of optics. Previous work show optical interconnects as a viable alternative to current electrical interconnects for off-chip interconnections due to higher bandwidth capacity and improved latency of the latter [5, 6, 7]. Moreover, optical connectors are much denser than the electrical connectors and in the same area they can provide much higher connector count [8]. Transmission of high frequency signals through electrical wires is limited due to high frequency attenuation characteristics, which is not the case with optical communication. Long off-chip electrical interconnects will also consume more power due to signal processing and equalization, which can be eliminated with the use of optical waveguides [9].

systems with high performance and low power dissipation. Our solution envisions a novel silicon interposer with electrical, optical, and fluidic (trimodal) interconnects and through-silicon vias (TSVs). Fig. 3 shows a schematic of a highly scalable integrated system using our silicon interposer technology with polymer-clad electrical TSVs, optical TSVs and fluidic TSVs. Fig. 4 shows a cross sectional view of the above system with electrical and optical TSVs side by side.

The electrical TSVs in the silicon interposer enable power and signal delivery from the motherboard to the chips stacked on top of the interposer. Optical TSVs in the silicon interposer can help provide ultra-high bandwidth communication between chips on different silicon interposers. The fluidic TSVs enable a coolant to be routed, for example, from the motherboard, to the chips on the silicon interposer. L. Kaun, et. al. and S. Ryu, et. al. have shown considerable reduction in thermal stress around electrical TSVs by using a thick polymer buffer between the copper and the silicon [10, 11]. D. S. Tezcan, et. al. have shown fabrication of TSVs with 35 μm outer diameter, 25 μm inner diameter (5 μm thick annulus shaped polymer liner) and 50 μm height [12]. Use of optical holes for communication between chips to achieve high bandwidth communication has been shown by [13, 14]. Use of integrated liquid cooling to address the increasing power consumption in microprocessors has been shown by [15, 16, 17]. However all these are independent solutions using disparate fabrication processes. We present an integrated solution to fabricate all of these critical interconnect solutions on the same “thick” (for mechanical stiffness) silicon interposer. We envision direct mounting of the silicon interposer on the motherboard. While this presents a large coefficient of thermal expansion (CTE) mismatch problem between the interposer and the motherboard, a number of innovations are currently being pursued to address this. Fig. 5 shows the step by step integration of the envisioned system showing components at each stratum.

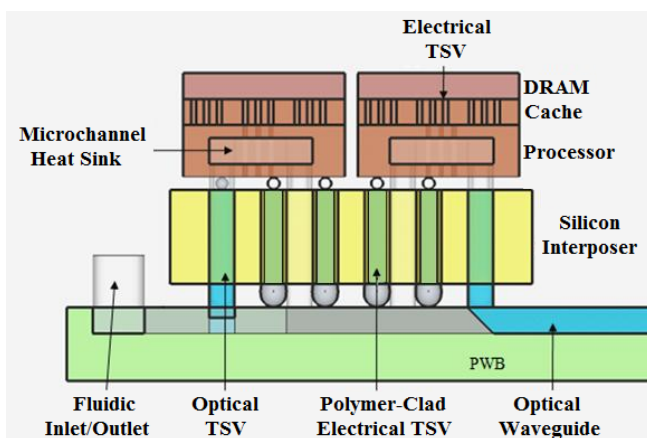


Fig. 4 Cross sectional view of silicon interposer showing electrical and optical TSVs side by side

To address the increasing computation demand in high performance computing systems, it is needed to build new

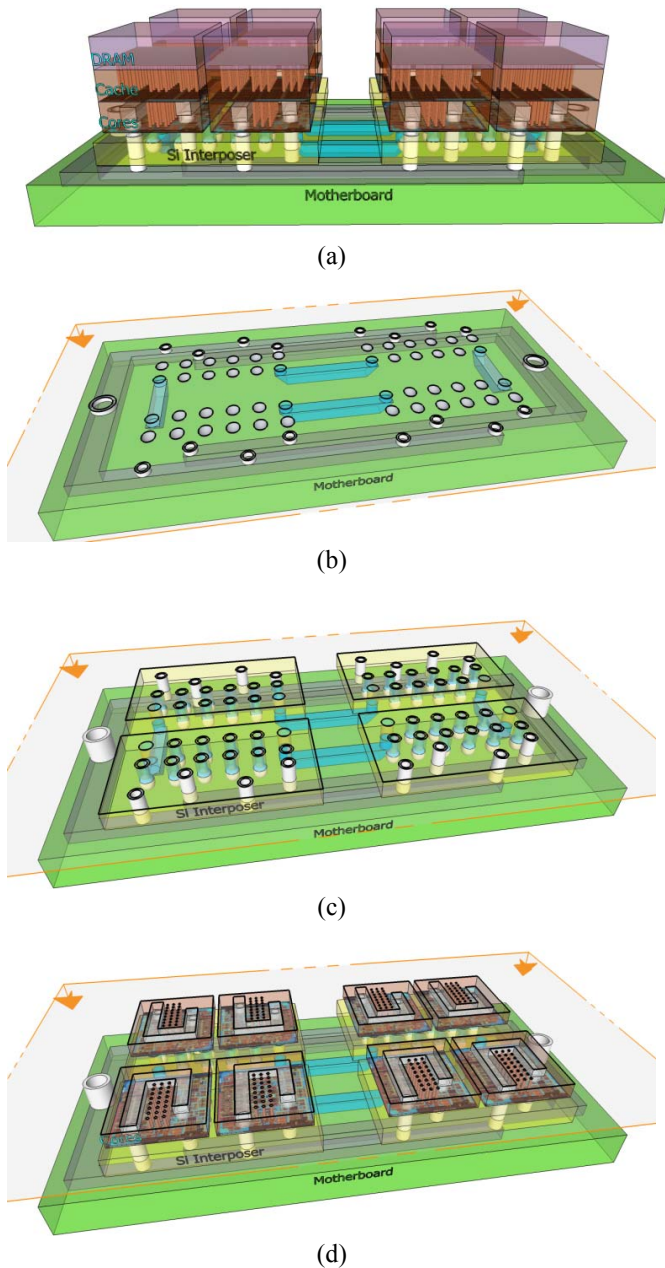


Fig. 5 (a) Schematic showing integration of silicon interposer in a 3D system. (b) Layout of motherboard showing fluidic inlets and outlets with fluidic channels (the outer channels in grey) and optical waveguides with pillars (blue). (c) Layout of silicon interposer with trimodal interconnects. (d) Layout showing multiple chips with fluidic heat sink channels on a silicon interposer

II: Polymer-clad Electrical TSVs

In an integrated 3D system, by including a thick silicon interposer between the Printed Wiring Board (PWB) and stacks of processor cores and memory, fine pitch wiring can be obtained using metallization layers on top of the silicon interposer using existing photolithography techniques. This leads to an increase in interconnect densities compared to

organic or ceramic substrates. Copper filled TSVs in the silicon interposer can be used to connect the 3D stack to the PWB. But the CTE of copper is approximately 7 times higher than that of silicon. This leads to higher stress in the silicon surrounding the copper TSV. It also leads to cracks in the copper at the TSV edges due to high stress concentration [18]. One solution to this problem is to build electrical TSVs with a thick polymer cladding around the copper conductor [10, 11]. In this work, we use SU-8 as the cladding, though we have also used other dielectrics for the TSV cladding. The Young's modulus of SU-8 is 4 GPa, which is low compared to that of silicon (130 GPa) and copper (110 GPa). The thick polymer cladding also reduces TSV capacitance, and thus, improves electrical characteristics.

Two masking steps are used for the fabrication of the polymer-clad TSVs. As shown in Fig. 6, silicon dioxide is first deposited on the back of a 'thick' silicon wafer. Then using anisotropic etching, TSVs are etched using a photoresist mask. After etching the vias, a mesh pattern is formed in the silicon dioxide suspended membrane on the back side of the vias [19]. Next, SU-8 is spin coated and optically defined using photolithography to obtain SU-8-clad vias.

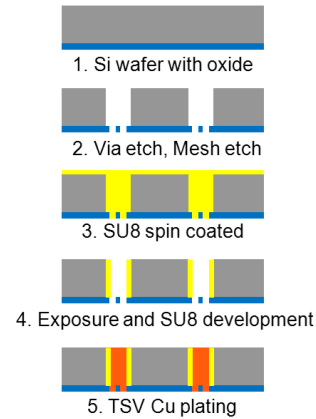


Fig. 6 Fabrication process for SU-8-clad TSVs

Due to the presence of a mesh at the bottom of the vias, void-free filling of the spin-coated SU-8 is obtained in the etched vias. Once the SU-8 cladding is photo-defined, titanium and copper seed layers are deposited on the mesh side. The titanium layer is used to obtain adhesion between the copper and the silicon. After seed layer deposition, the mesh is pinched-off using copper electroplating. Once the mesh is pinched-off, a bottom-up copper electroplating of the TSVs is done. Overburden copper at the end of the bottom-up electroplating is removed using chemical mechanical polishing (CMP).

SU-8-clad TSVs with 120 μm outer diameter, 80 μm inner diameter (20 μm thick annulus shaped SU-8 cladding) and 390 μm tall were fabricated (Fig. 7 and Fig. 8). The inner diameter of TSVs meets ITRS projection of 80 μm diameter vias for interposers for high performance computing systems for the year 2017.

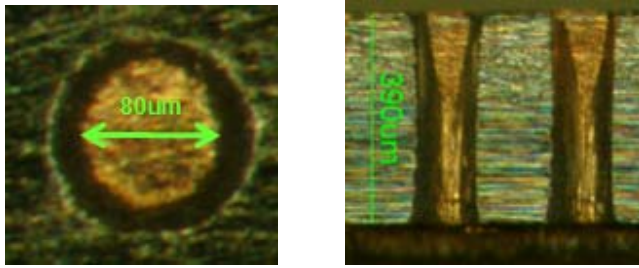


Fig. 7 Top view (left) and cross-section view (right) of SU-8-clad TSVs

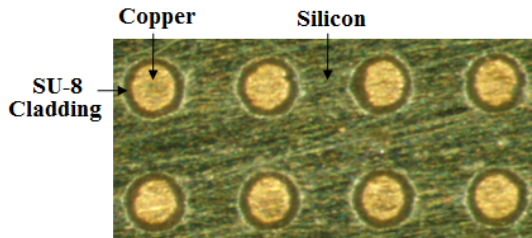


Fig. 8 Array of eight SU-8-clad TSVs

Once the fabrication is done, resistance measurements of the polymer-clad TSVs are done using the four-point resistance measurement method (Fig. 9). Fig. 10 shows the distribution of polymer-clad TSVs across different ranges of measured resistance values for 20 SU-8-clad TSVs. The average value of measured resistance is 2.81 mΩ.

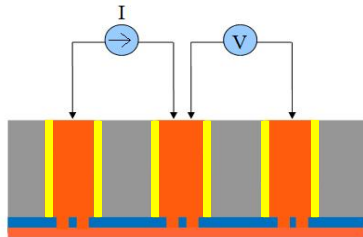


Fig. 9 Four-point resistance measurement of electrical TSVs

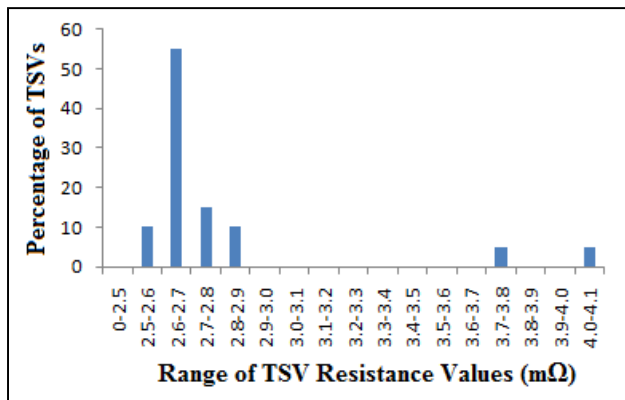


Fig. 10 Percentage of polymer-clad TSVs for the different ranges of measured TSV resistance values

III: Optical TSVs

SU-8 has good optical transmission characteristics in the window of 850 nm wavelength and hence is a suitable material for optical vias [20]. Chen Y., et. al., have shown the use of SU-8 polymer for fabrication of optical interconnects [21]. Optical TSVs are fabricated simultaneously while fabricating the electrical TSVs using the same cladding polymer SU-8 (Fig. 11). Since SU-8 is negative tone, the SU-8-filled optical TSVs are exposed to UV light during photolithographic patterning of the SU-8 cladding of electrical TSVs. As a result, SU-8 is not developed from the optical TSVs during SU-8 development. The optical TSVs are designed to act as a light pass-through. To enable this, we designed a structure similar to some extent of an optical fiber. The optical TSV has a cladding layer of silicon dioxide (~ 2 μm thicknesses) and core of SU-8 polymer ~ 118 μm in diameter. The refractive indices of silicon dioxide and SU-8 are 1.54 and 1.588 (at 830nm wavelength) respectively. We have fabricated wafer samples with optical TSV height ranging from 300-400 μm. With the right design, the TSV can act as an aperture and fabrication of lens at each end can further enhance the coupling.

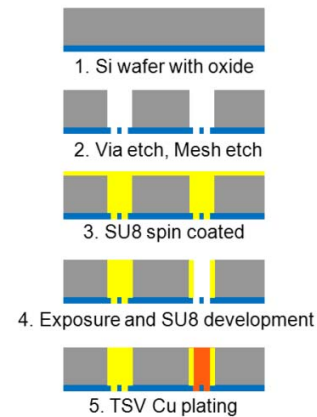


Fig. 11 Simultaneous fabrication of electrical and optical TSVs

The losses in the optical TSVs are measured with the help of the experimental setup shown in Fig. 12, Fig. 13 and Fig. 14. A single mode optical fiber (diameter 125 μm, 8 μm core) is connected to a laser source of 830 nm which acts as input to the optical TSV. At the other end of the TSV, a photo-detector is held close to the wafer to measure the output power (P_{out}) from the TSV. Initially the wafer is removed and the optical fiber is held at the photo-detector to measure the input power (P_{in}) to the optical TSV. Optical loss is calculated as $Loss(dB) = 10 \log_{10}(P_{in}/P_{out})$. We measured the losses by reversing the wafer and still the average losses were found to be the same, thus making it symmetric with respect to injection of light. For a 390 μm wafer, averaged losses over large number of TSVs and across different sets were measured to be 0.59 dB with a standard deviation of 0.15 dB.

All the measurements were carefully done so as to have no impact of the ambient light. We also measured the optical losses through an empty via to compare it against a polymer via. The averaged losses through the empty TSVs are slightly lower (0.53 dB with standard deviation of 0.27 dB) than that

of the polymer TSVs. The graph in Fig. 15 shows the distribution of optical TSVs across different range of losses. The optical losses in the polymer TSVs can be attributed to the following factors: material loss in the TSV, reflection losses due to imperfect coupling at the fiber-via and the via-photo detector surfaces and the losses due to conversion of single mode light into multi-mode light as it passes from the fiber to the TSV. One advantage of the optical polymer TSVs is that it makes the surface of the interposer flat which eases subsequent fabrication steps. The optical TSVs in the interposer can also be kept hollow as shown in [22].

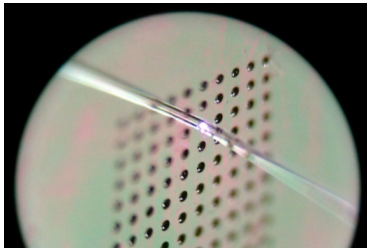


Fig. 12 Microscope image showing optical fiber aligned with one of the optical TSVs

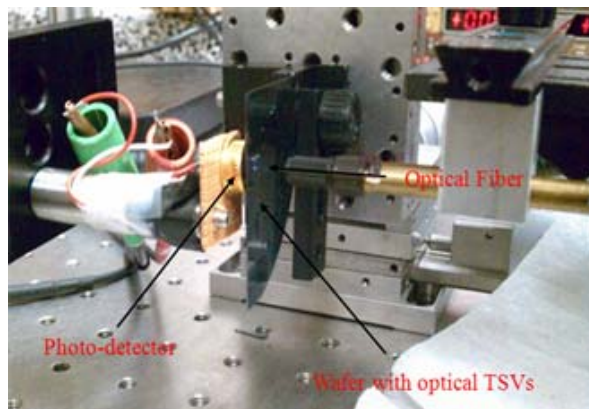


Fig. 13 Optical setup to measure the losses of the optical TSVs

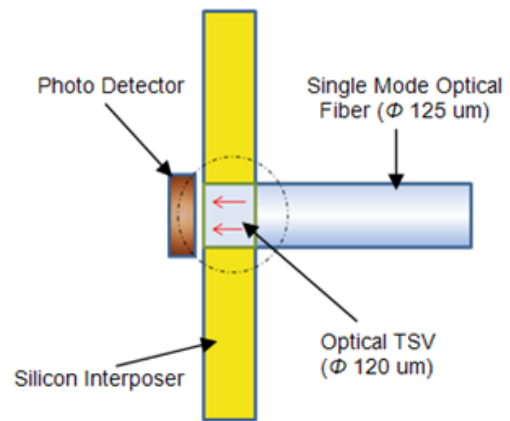


Fig. 14 Schematic showing setup to measure the losses of the optical TSVs

Empirically, we find that the material losses are negligible and the majority of losses are accounted by mode conversion and reflection. Losses due to reflection can be up to 0.3 dB based on Fresnel's reflection formula which can be eliminated with the use of a sophisticated index matching gel. Previous work on optical holes by Keiko Oda et. al. at Kyocera Corporation and Yutaka Takagi et. al. at NGK Spark Plug Co. have measured insertion losses of 1.4 dB and 4 dB respectively for similar sized vias [13, 14].

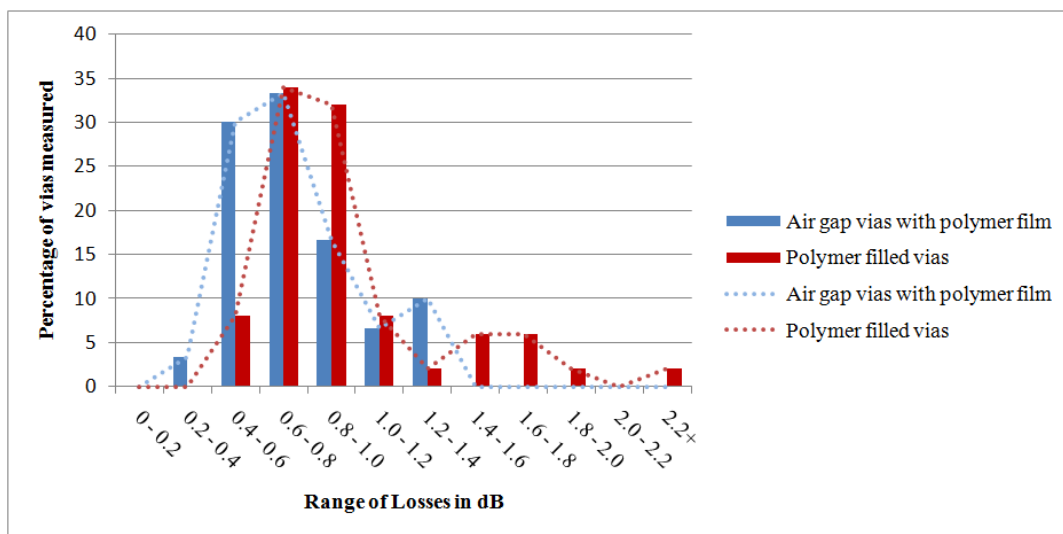


Fig. 15 Loss distribution of optical TSVs

The following images in Fig. 16 show cross-sectional views of the optical TSVs.

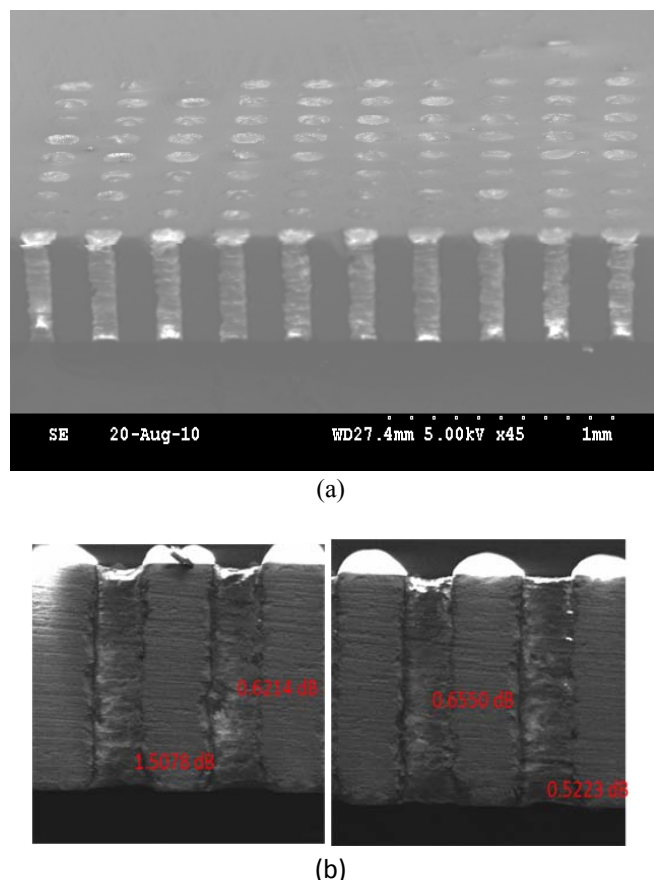


Fig. 16 (a) Cross-sectional view of the optical TSVs. (b) Each image shows cross sectional view of two optical TSVs along with the measured optical losses

IV: Fluidic TSVs

Fabrication process for the fluidic TSVs is similar to that of the polymer-clad electrical TSVs in Fig. 6. Fluidic TSVs can be fabricated using the same cladding (for insulation purpose) as that of the polymer-clad electrical TSVs. The copper electroplating is prevented for the fluidic TSVs to leave behind empty polymer-clad TSVs. This can be done by preventing silicon dioxide etching (during step 2 of Fig. 6) at the bottom of the TSVs. Fig. 17 shows a schematic of electrical, optical and fluidic TSVs fabricated side by side on a silicon interposer.

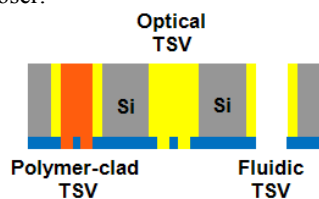


Fig. 17 Simultaneous fabrication of electrical, optical and fluidic TSVs

Due to the low heat transfer coefficient of forced air cooling, the low thermal resistance requirement (< 0.2 C/W) projected by the ITRS for high-performance single chips in 2018 will necessitate the use of advanced cooling, such as single-phase or two-phase liquid cooling. The hollow polymeric via enables connection and delivery of liquid coolant to microchannel heat sinks embedded in the silicon chips as shown earlier in Fig. 4 and Fig. 5(d). Previous work in [23, 24, 25] have successfully demonstrated the use of microchannel heat sinks embedded in silicon chips for integrated cooling.

V: Conclusion

The paper proposes the concept of trimodal interconnects for silicon interposers. The polymer-clad electrical TSVs in the silicon interposer help deliver power and signal from motherboard to chips stacked on top of the interposer. The optical TSVs help provide ultra-high bandwidth of communication among different silicon interposers and the fluidic TSVs help transfer the coolant through the silicon interposer to the top chips to achieve a system level cooling.

Acknowledgments

The work was supported by the US Department of Defense Maryland Procurement Office under contract number H98230-09-C-0375. The authors are grateful to Suzanne Bock for help with the fabrication of the TSVs and Fan Shu-Hoy and Dr. G.K. Chang for help with the optical measurement setup.

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